

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
Before the Board of Patent Appeals and Interferences

In re Patent Application of

WALLES

Serial No. 09/902,804

Filed: July 12, 2001

Title: MEDIA STREAM DELAY MONITORING FOR NODE



Atty Dkt. 2380-380

C# M#

TC/A.U.: 2664

Examiner: Lee, A.C.C.

Date: November 1, 2005

JAF
JFW

Commissioner for Patents

P.O. Box 1450

Alexandria, VA 22313-1450

Sir:

Correspondence Address Indication Form Attached.

NOTICE OF APPEAL

Applicant hereby **appeals** to the Board of Patent Appeals and Interferences from the last decision of the Examiner twice/finally rejecting \$500.00 (1401)/\$250.00 (2401) \$ 500.00 applicant's claim(s).

An appeal **BRIEF** is attached in the pending appeal of the above-identified application

\$500.00 (1402)/\$250.00 (2402) \$

Credit for fees paid in prior appeal without decision on merits

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A reply brief is attached in triplicate under Rule 41.41

(no fee)

Pre-Appeal Brief Request for Review form attached.

Petition is hereby made to extend the current due date so as to cover the filing date of this paper and attachment(s)

One Month Extension \$120.00 (1251)/\$60.00 (2251)

Two Month Extensions \$450.00 (1252)/\$225.00 (2252)

Three Month Extensions \$1020.00 (1253)/\$510.00 (2253)

Four Month Extensions \$1590.00 (1254)/\$795.00 (2254) \$ 450.00

"Small entity" statement attached.

Less month extension previously paid on

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TOTAL FEE ENCLOSED \$ 950.00

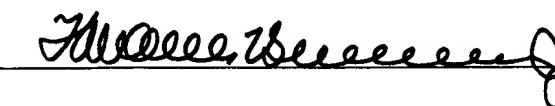
Any future submission requiring an extension of time is hereby stated to include a petition for such time extension.

The Commissioner is hereby authorized to charge any deficiency, or credit any overpayment, in the fee(s) filed, or asserted to be filed, or which should have been filed herewith (or with any paper hereafter filed in this application by this firm) to our **Account No. 14-1140**. A duplicate copy of this sheet is attached.

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11/02/2005 JADD01 00000012 09902804
NIXON & VANDERHYE P.C.
By Atty: H. Warren Burman, Jr., Reg. No. 29,366

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Signature: 

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

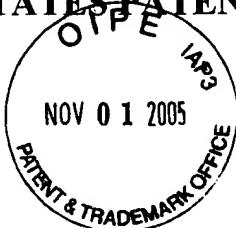
In re Patent Application of

WALLES

Serial No. 09/902,804

Filed: July 12, 2001

For: MEDIA STREAM DELAY MONITORING FOR NODE



Confirm. No.: 6649

Atty. Ref.: 2380-380

TC/A.U.: 2664

Examiner: Lee, A.C.C.

November 1, 2005

MAIL STOP AF
Commissioner for Patents
P. O. Box 1450
Alexandria, VA 22313-1450

Sir:

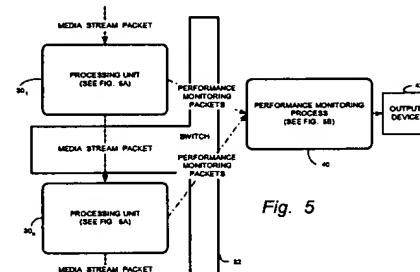
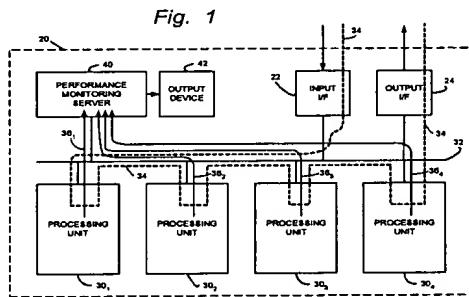
PRE-APPEAL BRIEF REQUEST FOR REVIEW

In conjunction with the Notice of Appeal filed simultaneously herewith, and in accordance with the Pre-Appeal Brief Conference Pilot Program announced by OG 12 July 2005, Applicant respectfully requests that a panel of examiners formally review the legal and factual basis of the prior art rejections of the captioned application.

Selected Comments Concerning Applicant's Independent Claims

Independent claim 1 concerns a node of a packet switching network which handles a media stream of packets. The node comprises both a processing chain and a performance monitoring unit. The processing chain comprises plural processing units through which a packet of the media stream is routed. Each of the plural processing units generates an intra-node performance monitoring packet which includes an indication of time spent by the packet of the media stream in the respective processing unit. The performance monitoring unit receives the intra-node performance monitoring packets generated by the respective plural processing units and uses contents of the intra-node performance monitoring packets to provide an indication of delay in the node for the

media stream. Independent claim 10 is essentially a method analogue of apparatus claim 1. Applicant shows an example chain of processors (30) and an example performance monitoring unit (40) in Figs. 1 and 5, copied below.



The Rejection and sole applied reference (Radha)

Claims 1-19 stand rejected under 35 USC §102(e) as being anticipated by U.S. Patent 6,700,893 to Radha et al. The first paragraph of column 16 of Radha appear to summarize the Radha teaching:

"Delay budget controller 138 monitors ITD buffer 132 to detect the absence of expected packets. If a packet is not received after a minimum monitoring time, it is determined to be lost and a NACK message is sent to streaming video transmitter 110 (process step 615). Using the statistics gathered by real-time QoS characterization circuit 505, delay budget controller 138 calculates the probability distribution functions for round trip delay and delay jitter. Delay budget controller 138 also calculates the probability that a video packet has actually been lost when it was declared lost (process step 602)."

U.S. Patent Mar. 2, 2004 Sheet 1 of 4 US 6,700,893 B1

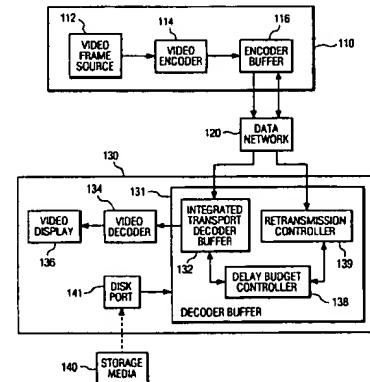


FIG. 1

The prior art rejections are traversed for various main reasons:

1. Radha does not teach or suggest the claimed processing chain

U.S. Patent 6,700,893 to Radha et al does not teach, e.g., a *processing* chain comprising plural *processing units* through which a packet of a media stream is routed. The fifth enumerated paragraph of the Final Office Action appears to allege that the Radha IDT buffers (132), delay budget controller (138), and re-transmission controller (139) are processing units (by virtue of being implemented in a personal computer (PC) or the like). Yet in such case these Radha elements (IDT buffers, delay budget controller, and re-transmission controller) are implemented by the same processor, and therefore are not plural processing units of a chain. Moreover, of the three elements identified in enumerated paragraph 5 of the Final Office Action, the Radha packets themselves only travel through ITD buffer 132. The Radha packets do not travel through plural separate processing units. Thus, the Radha packets do not travel through processing units of a chain.

In view of enumerated paragraph 5 of the Office Action, it appears that the Examiner is no longer asserting that Radha's "access units" are the alleged processors. As previously explained, Radha's "access units" are instead merely a grouping of packets in IDT buffer 132 (see the last full ¶ of col. 7 and the ¶ bridging col. 7 and col. 8 of Radha).

2. Radha does not generate distinct intra-node performance monitoring packets

Nor do any units through which the Radha packets may travel generate any further distinct packets which serve for intra-node performance monitoring. Radha has a buffer manager for monitoring delay in the one buffer. But the buffer itself is not a processor, nor does it generate separate packets for communicating "time spent" information to a performance monitoring unit. Radha's delay buffer controller 138 only "monitors" the level of data occupancy in ITD buffer 132. There is no mention of packet generation or transmission for such purpose. In fact, no unit of Radha appears to generate any such packets.

3. Radha's delay is overall network delay, not delay within a node

The delay of concern to Radha is not delay in the node itself, but overall network delay. Radha is essentially measuring delay to determine if a packet has been lost in the network. Radha's monitoring is totally different in its purpose and approaching, being essentially for the purpose of detecting missing data packets and potential underflow conditions for the purpose of requesting re-transmission as necessary (*see, e.g., col. 5, lines 65+*)

Therefore, not teaching or suggesting a chain of processing units, not having any processing unit which generates an intra-node performance monitoring packet, and not being concerned with intra-node delay, Radha lacks many significant aspects of Applicant's claim and provides no sustainable basis for denial of patentability.

The Commissioner is authorized to charge the undersigned's deposit account #14-1140 in whatever amount is necessary for entry of these papers and the continued pendency of the captioned application.

Respectfully submitted,
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